IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims

1. (Canceled)

2. (Canceled)

3. (Original) A timing error detection circuit for detecting a timing error of symbols arranged at a predetermined symbol cycle T included in a signal, comprising:

a sampling circuit for sampling said signal at a frequency equal to four times of a symbol rate;

an amplitude detection circuit for detecting an amplitude at said sampled position in said signal; and

a detection circuit for detecting a direction and amount of said timing error based on the large or small relationship and the difference of said detected amplitude at time "T/4" and the detected amplitude at time "3T/4" when assuming a symbol appears at times "0" and "T".

4. (Original) A timing error detection circuit as set forth in claim 3, wherein said signal is a phase shift modulated signal.

5. (Original) A timing error detection circuit for detecting a timing error of symbols arranged at a predetermined symbol cycle T included in a signal, comprising:

a sampling circuit for sampling at a frequency equal to double of a symbol rate;

an interpolation circuit for generating data at time "T/4" by using sampled data at time "0" and "T/2", and generating data at time "3T/4" by using said sampled data at time "T/2" and data on time "T" when assuming a symbol appears at times "0" and "T";

an amplitude detection circuit for detecting an amplitude of said signal at the position from data at said time "T/4" and time "3T/4"; and

a detection circuit for detecting a direction and amount of said timing error based on the large or small relationship and the difference of the amplitude at said time "T/4" and the amplitude at said time "3T/4".

6. (Original) A timing error detection circuit as set forth in claim 5, wherein said signal is a phase shift modulated signal.

7. (Canceled)

8. (Canceled)

9. (Original) A demodulation circuit, comprising:

a symbol timing reproduction circuit for detecting a timing error of symbols arranged at a predetermined symbol cycle included in a signal and reproducing a symbol timing of said signal based on the detected timing error;

a carrier reproduction circuit for performing carrier reproduction of the signal wherein said symbol timing is reproduced; and

a symbol decode circuit for decoding said symbol included in said carrier reproduced signal:

and wherein:

said symbol timing reproduction circuit comprises:

a sampling circuit for sampling said signal at a frequency equal to four times of a symbol rate;

an amplitude detection circuit for detecting an amplitude at said sampled position in said signal;

a detection circuit for detecting a direction and amount of said timing error based on sizes and difference of said detected amplitude at time "T/4" and the detected amplitude at time "3T/4" when assuming a symbol appears at times "0" and "T"; and

an interpolation circuit for reproducing the symbol timing by performing interpolation processing on said signal based on said detected timing error.

10. (Original) A demodulation circuit as set forth in claim 9, wherein said signal is a phase shift modulated signal.

11. (Original) A demodulation circuit, comprising:

a symbol timing reproduction circuit for detecting a timing error of symbols arranged at a predetermined symbol cycle included in a signal and reproducing a symbol a symbol timing of said signal based on the detected timing error;

a carrier reproduction circuit for performing carrier reproduction of the signal wherein said symbol timing was reproduced; and

a symbol decode circuit for decoding said symbol included in said carrier reproduced signal;

and wherein:

said symbol timing reproduction circuit comprises:

a sampling circuit for sampling said signal at a frequency equal to double of a symbol rate;

a first interpolation circuit for generating data at time "T/4" by using said sampled data at time "0" and "T/2", and generating data at time "3T/4" by using said sampled data at time "T/2" and data at time "T" when assuming a symbol appears at times "0" and "T";

an amplitude detection circuit for detecting an amplitude of said signal at the position from data on said time "T/4" and data at said time "3T/4";

a detection circuit for detecting a direction and amount of said timing error based on the large or small relationship and the difference of an amplitude at said time "T/4" and an amplitude at said time "3T/4"; and

a second interpolation circuit for reproducing a symbol timing by performing interpolation processing on said signal based on said detected timing error.

12. (Original) A demodulation circuit as set forth in claim 11, wherein said signal is a phase shift modulated signal.

13. (Canceled)

14. (Canceled)

15. (Original) A timing error detection method for detecting a timing error of symbols arranged at a predetermined symbol cycle T included in a signal, including the steps of:

sampling said signal at a frequency of four times a symbol rate;

detecting an amplitude at said sampled position in said signal; and

detecting a direction and size of said timing error based on sizes and difference of said detected amplitude at time "T/4" and the detected amplitude at time "3T/4" when assuming a symbol appears at times "0" and "T".

16. (Original) A timing error detection method as set forth in claim 15, wherein said signal is a phase shift modulated signal.

17. (Original) A timing error detection method for detecting a timing error of symbols arranged at a predetermined symbol cycle T included in a signal, including the steps of:

sampling at a frequency equal to double of a symbol rate;

generating data at time "T/4" by using said sampled data at time ?0" and data at time "T/2" when assuming a symbol appears at times "0" and "T";

generating data at time "3T/4" by using said sampled data at time "T/2" and data on time "T";

detecting an amplitude of said signal at the position from data at said time "T/4" and time "3T/4"; and

detecting a direction and size of said timing error based on the large or small relationship and the difference of the amplitude at said time "T/4" and the amplitude at said time "3T/4".

18. (Original) A timing error detection method as set forth in claim 17, wherein said signal is a signal subjected to phase shift modulation.

19. (Canceled)

20. (Canceled)

21. (Original) A demodulation method, including the steps of:

sampling said signal including symbols arranged at a predetermined symbol cycle at a frequency equal to four times of a symbol rate;

detecting an amplitude at said sampled position in said signal;

detecting a direction and size of said timing error based on the large or small relationship and the difference of said detected amplitude at time "T/4" and said detected amplitude at time "3T/4" when assuming a symbol appears at times "0" and "T";

reproducing a symbol timing by performing interpolation processing on said signal based on said detected timing error;

performing carrier reproduction of the signal wherein said symbol timing is reproduced; and

decoding said symbol included in said carrier reproduced signal.

22. (Original) A demodulation method as set forth in claim 21, wherein said signal is a phase shift modulated signal.

23. (Original) A demodulation method including the steps of:

sampling a signal including symbols arranged at a predetermined symbol cycle at a frequency equal to double of a symbol rate;

generating data at time "T/4" by using said sampled data at time "0" and data at time "T/2" when assuming a symbol appears at times "0" and "T";

generating data at time "3T/4" by using said sampled data at time "T/2" and data at time "T";

detecting an amplitude of said signal at the position from data at said time "T/4" and data at time "3T/4"; and

detecting a direction and amount of said timing error based on the large and small relationship and difference of the amplitude of said time "T/4" and the amplitude at said time "3T/4";

reproducing the symbol timing by performing interpolation processing on said signal based on said detected timing error;

performing carrier reproduction of the signal wherein said symbol timing is reproduced; and

decoding said symbol included in said carrier reproduced signal.

24. (Original) A demodulation method as set forth in claim 23, wherein said signal is a signal subjected to phase shift modulation.